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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/801,843	03/09/2001	Hiroaki Fukuda	203930US6	6321

22850 7590 04/19/2004

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ART UNIT	PAPER NUMBER
2183	14

DATE MAILED: 04/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PRE

Office Action Summary	Application No. 09/801,843	Applicant(s) FUKUDA ET AL.	
	Examiner Barry J. O'Brien	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004 and 17 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4.7-13*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-49 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Declaration as received on 7/23/2001, IDS as received on 3/09/2001, Priority Papers as received on 3/09/2001, Change of Address as received on 4/03/2003, IDS as received on 5/12/2003, IDS as received on 8/08/2003, IDS as received on 11/04/2003, IDS as received on 11/17/2003, IDS as received on 12/19/2003, IDS as received on 1/20/2004, and IDS as received on 2/17/2004.

Information Disclosure Statement

3. The Examiner has considered the IDS statements containing references to co-pending/related applications as filed on 3/9/01, 5/12/03, 8/8/03, 11/4/03, 11/17/03, 12/19/03, 1/20/04 and 2/17/04. However, the Examiner requests that the Applicant amend the specification to include the cited co-pending applications in a section describing co-pending and related applications (see 37 CFR 1.78 and MPEP 201.11).

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

6. The disclosure is objected to because of the following informalities:

a. The specification is generally narrative and indefinite, failing to conform to current U.S. practice. It appears to be a literal translation into English from a foreign document and is replete with grammatical and idiomatic errors.

Appropriate correction is required.

Claim Objections

7. Claims 1-17 and 22-38 are objected to because of the following informalities:

a. A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim. A claim that depends from a dependent claim should not be separated by any claim that does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n). See claims 1-17 and 22-38, specifically groups of claims such as 1-6, where claim 4 improperly depends on claim 2, while claim 3 depends on claim 1.

b. Regarding claim 10, the limitation "The image processing apparatus comprising" is stated on its first line. Because this is an independent claim, please correct the claim language to read "An image processing apparatus comprising" so as to

more clearly define itself as an independent claim and provide the correct antecedent basis. See also the same issue in claim 31.

c. Regarding claim 5, the limitation "a resistor" is recited on its fourth line. Although a "resistor" is mentioned in the specification, the Examiner believes that this is meant to be a "register", which would make more sense in relation to the application and the manner in which the "resistor" is described as being used in the specification. Please correct the claim language to read "a register". See a similar problem in claim 26 also.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1-49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

11. Claim 1 recites the limitation "given data" on its fourth line. There is insufficient antecedent basis for this limitation in the claim. See also claim 22 for a similar problem.

12. Claim 1 recites the limitation "the same instruction" on lines 7-8 and 26 of the claim. There is insufficient antecedent basis for this limitation in the claim. See also claim 22 for a similar problem.

13. Claim 2 recites the limitation "the instruction" on lines 2-3 of the claim. There is insufficient antecedent basis for this limitation in the claim. See also claim 23 for a similar problem.

14. Claim 7 recites the limitation "an image data control unit connected to" on its second line. It is unclear what the image data control unit is connected to, if anything. Please correct the claim language to more clearly point out how the image data control unit is connected to the rest of the system claimed in claim 7. See also claims 8 and 28-29 for similar problems.

15. Claim 7 recites the limitations "that receives" and "that transmits" on lines 9 and 14 of p.109 of the instant application. It is unclear from the claim language what is doing the receiving and transmitting, as it could be read to be any of the image data control unit, the image memory control unit, or the image processing unit. Please correct the claim language to more clearly define the relationship of the claimed elements. See also claims 8 and 28-29 for similar problems.

16. Regarding claims 7-8, 10, 28-29, 31, 45 and 49, the phrase "such as" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

17. Claim 9 recites the limitation "the image data control unit" on line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim. See also claim 30 for a similar problem. See also claims 11, 30 and 32 for similar problems.

18. Claim 9 recites the limitation "via the image data control unit" on line 3 of the claim. It is unclear whether only the image writer is connected to the image memory control unit via the image data control unit, or if the other units in the alternative statement (the image processing unit and the image reader) can (or are) connected to the image memory control unit via the image data control unit also. Please correct the claim language to more clearly define the relationship of the claimed elements. See also claims 11, 30 and 32 for similar problems.

19. Claim 45 recites the limitation "relating to" on line 19 of p.138 of the instant application. This phrase renders the claim indefinite, as it is unclear in what manner and to what extent the "information" relates to the "contents of processing". See also claim 49 for a similar problem.

Claim Rejections - 35 USC § 102

20. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

21. Claims 1-4, 6, 22-25, 27, 43-44 and 48 are rejected under 35 U.S.C. 102(e) as being anticipated by Morton, U.S. Patent No. 6,088,783.

22. Regarding claims 1, 22, 43 and 48, taking claim 1 as exemplary, Morton has taught a SIMD type processor (see Col.5 lines 37-40) comprising:

a. A parallel processing unit (see 110-113 of Fig.1) that carries out a parallel processing using a plurality of arithmetic units which carry out an arithmetic processing to given data (see Col.24 lines 24-30),

b. A data providing unit (109 of Fig.1) that provides data to be arithmetically processed to the parallel processing unit (see Col.21 lines 40-53),

c. An instruction providing unit (105 of Fig.1) that provides the same instruction for carrying out the arithmetic processing to each of the arithmetic unit (see Col.16 line 34 – Col.17 line 24),

d. An input unit (106 of Fig.1) that inputs an interruption request for carrying out other parallel processing by interrupting a parallel processing currently carried out by the parallel processing unit (see Col.17 line 37 – Col.18 line 8),

e. A decision unit (106 of Fig.1) that makes a decision as to whether a parallel processing requested by the interruption request input from the input unit is to be carried out or not (see Col.17 lines 54-59). Here, the interrupt controller makes a decision whether to process an interrupt based on its priority.

f. A suspending (106 of Fig.1) unit that suspends a parallel processing currently being carried out by the parallel processing unit when the decision unit has decided that the interruption processing is to be carried out (see Col.17 lines 60-66),

g. A control unit (106 of Fig.1) that controls the data providing unit and the instruction providing unit so as to provide data to be arithmetically processed by the interruption processing to the parallel processing unit in place of the parallel

processing suspended by the suspending unit and to provide the same instruction necessary for carrying out the interruption processing to each of the arithmetic units (see Col.17 line 54 – Col.18 line 8). Here, an interrupt vector is loaded and subsequently executed following the suspension of the normal execution.

23. Claims 22, 43 and 48 are nearly identical to claim 1. Claim 22 differs in the limitations being comprised within a parallel processing apparatus instead of a SIMD type processor as recited in claim 1. However, a SIMD type processor is a parallel processing apparatus (see Col.5 lines 37-40 and Col.24 lines 24-30). Claim 43 differs in the limitations being comprised within a method, but the method encompasses the same scope as claim 1. Claim 48 differs in the limitations being comprised on a computer readable medium, but Morton has taught its instructions being stored on a computer readable medium for executing (see Col.6 lines 33-45 and Col.14 lines 39-61). Therefore, claims 22, 43 and 48 are rejected for the same reasons as claim 1.

24. Regarding claims 2 and 23, taking claim 2 as exemplary, Morton has taught the SIMD type processor according to claim 1, further comprising an instruction storing unit (104 of Fig.1) that stores the instruction (see Col.14 lines 39-61).

25. Claim 23 is nearly identical to claim 2, differing in its parent claim, but encompassing the same scope as claim 2. Therefore, claim 23 is rejected for the same reasons as claim 2.

26. Regarding claims 3, 24 and 44, taking claim 3 as exemplary, Morton has taught the SIMD type processor according to claim 1, further comprising:

a. A storing unit (see 105 of Fig.1) that stores suspension information consisting of data and an instruction at a point of time when a parallel processing has been suspended by the suspending unit (see Col.17 line 61 – Col.18 line 3),

b. A detecting unit that detects whether the interruption processing has been finished or not (see Col.18 lines 4-8). Here, the interrupt controller detects when the interrupt is finished processing so that normal execution can resume.

c. A transmission unit that transmits the suspension information stored by the storing unit to an original position when detecting unit has detected a finish of the interruption processing (see Col.17 line 61 - Col.18 line 8). Here, normal program execution is resumed using the address of the next normal instruction stored prior to interrupt processing.

27. Claims 24 and 44 are nearly identical to claim 3, differing only in their parent claims, but encompassing the same scope as claim 3. Therefore, claims 24 and 44 are rejected for the same reasons as claim 3.

28. Regarding claims 4 and 25, taking claim 4 as exemplary, Morton has taught the SIMD type processor according to claim 2, further comprising:

a. A program counter (601 of Fig.6),

b. An accumulator (812 of Fig.8) that is used in the arithmetic units (see Col.25 line 59 – Col.26 line 23),

c. Wherein the program counter assigns an instruction stored by the instruction storing unit, and each arithmetic units carries out the arithmetic processing using the accumulator (see Col.19 lines 15-27).

29. Claim 25 is nearly identical to claim 4, differing in its parent claim, but encompassing the same scope as claim 4. Therefore, claim 25 is rejected for the same reasons as claim 4.

30. Regarding claims 6 and 27, taking claim 6 as exemplary, Morton has taught the SIMD type processor according to claim 3, wherein the storing unit stores various parameter data that are necessary for the arithmetic processing carried out by the arithmetic units (see Col.17 line 61 – Col.18 line 3). Here, the processor status word and the PC are saved, both of which are required to process subsequent instructions.

31. Claim 27 is nearly identical to claim 6, differing in its parent claim, but encompassing the same scope as claim 6. Therefore, claim 27 is rejected for the same reasons as claim 6.

Claim Rejections - 35 USC § 103

32. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

33. Claims 5 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morton, U.S. Patent No. 6,088,783, in further view of Short, *Embedded Microprocessor Systems Design: An Introduction Using the Intel 80C188EB*.

34. Regarding claims 5 and 26, taking claim 5 as exemplary, Morton has taught the SIMD type processor according to claim 3, further comprising:

a. A program counter (601 of Fig.6),

b. An accumulator (812 of Fig.8) and a register (807 of Fig.8) that are used in the arithmetic units (see Col.25 line 59 – Col.26 line 23).

c. A data register that stored data provided by the data providing unit (see Vector Register Bank of Fig.9). Here, all data stored in the vector register banks inherently has been provided by the data providing unit, as all data that gets to the vector processors must go through the crossbar switch (see Col.21 lines 40-53).

d. Wherein the suspension information consists of a program counter value (601 of Fig.6) and a register (807 of Fig.6) used in the arithmetic units at a point of time when a parallel processing has been suspended by the suspending unit (see Col.17 lines 54-66).

35. Morton has not explicitly taught wherein the SIMD type processor

a. Wherein the suspension information further consists of the contents of the accumulator and data stored in the data register.

36. However, Short has taught that when executing a context switch due to an interrupt that all information needed to correctly resume the task's execution following the interrupt must be saved, including registers (see Short, p.468-469). Because the accumulator is a register (see Morton, Col.24 line 44), one of ordinary skill in the art would have found it obvious to modify the processor of Morton to further save the accumulator register and other data registers upon an interrupt so that the task's execution could be completely and correctly returned to following the interrupt service routine's processing.

37. Claims 7-17, 19-21, 28-38, 40-42, 45-47 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugiura et al., U.S. Patent No. 5,387,983, in further view of Morton, U.S. Patent No. 6,088,783.

38. Regarding claims 7 and 28, taking claim 7 as exemplary, Suguira has taught an image processing apparatus comprising:

a. An image data control unit (50 of Fig.3) connected to (see Col.15 lines 46-49),

b. An image memory control unit (20a of Fig.3) that controls an image reader (20 of Fig.3) that reads image data (see Col.14 line 53 – Col.15 line 4) and/or an image memory (59 of Fig.3) thereby to write/read image data and/or an image writer (70 of Fig.3) that writes image data onto a transcription sheet (see Col.18 lines 55-66). Here, because the claim is written in the alternative format, Suguira has met the limitation.

c. An image processing unit (64 of Fig.3) that carries out an image processing of image data (see Col.15 lines 59-61 and Col.16 lines 17-57) such as an editing of image data,

d. That receives at least third image data out of first image data that has been read by the image reader (see Col.15 lines 59-61 and Col.16 lines 17-57), second image data that has been read by the image memory control unit (see Fig.3), and said third image data that has been image processed by the image processing unit (see Col.16 lines 34-57). Here, the image processing unit (64 of Fig.3) can receive data from the image reader (20 of Fig.3), data read from the image memory control unit (which gets its data from the image reader), or from the image

processing unit itself, which requires the image processor to make multiple scans of the data in order to completely interpolate it (see Col.16 lines 34-57).

e. That transmits at least the third image data out of the first image data, the second image data, and the third image data, to the image memory control unit and/or the image processing unit and/or the image writer (70 of Fig.3) (see Col.18 lines 55-66). Here, because the claim is written in the alternative format, Suguira has met the limitation because the laser printer of Suguira is an image writer.

39. Suguira has not explicitly taught wherein at least the image processing unit has a SIMD type processor.

40. However, Morton has taught a SIMD type processor (see Col.5 lines 37-40) for improving the performance of image processing (see Col.1 lines 18-38) comprising:

a. A parallel processing unit (see 110-113 of Fig.1) that carries out a parallel processing using a plurality of arithmetic units which carry out an arithmetic processing to given data (see Col.24 lines 24-30),

b. A data providing unit (109 of Fig.1) that provides data to be arithmetically processed to the parallel processing unit (see Col.21 lines 40-53),

c. An instruction providing unit (105 of Fig.1) that provides the same instruction for carrying out the arithmetic processing to each of the arithmetic unit (see Col.16 line 34 – Col.17 line 24),

d. An input unit (106 of Fig.1) that inputs an interruption request for carrying out other parallel processing by interrupting a parallel processing currently carried out by the parallel processing unit (see Col.17 line 37 – Col.18 line 8),

e. A decision unit (106 of Fig. 1) that makes a decision as to whether a parallel processing requested by the interruption request input from the input unit is to be carried out or not (see Col. 17 lines 54-59). Here, the interrupt controller makes a decision whether to process an interrupt based on its priority.

f. A suspending (106 of Fig. 1) unit that suspends a parallel processing currently being carried out by the parallel processing unit when the decision unit has decided that the interruption processing is to be carried out (see Col. 17 lines 60-66),

g. A control unit (106 of Fig. 1) that controls the data providing unit and the instruction providing unit so as to provide data to be arithmetically processed by the interruption processing to the parallel processing unit in place of the parallel processing suspended by the suspending unit and to provide the same instruction necessary for carrying out the interruption processing to each of the arithmetic units (see Col. 17 line 54 – Col. 18 line 8). Here, an interrupt vector is loaded and subsequently executed following the suspension of the normal execution.

41. Therefore, one of ordinary skill in the art would have found it obvious to modify the image processor of Sugiura to be a SIMD type processor as taught by Morton so that the image processing that Suguira performs can performed at a much faster rate.

42. Claim 28 is nearly identical to claim 7. Claim 7 requires that the image processing unit have a SIMD type processor, while claim 28 requires that the image processing unit has a parallel processing apparatus. However, a SIMD type processor is a parallel processing

apparatus (see Col.5 lines 37-40 and Col.24 lines 24-30). Therefore, claim 28 is rejected for the same reasons as claim 7.

43. Regarding claims 8 and 29, taking claim 8 as exemplary, Sugiura has taught an image processing apparatus comprising:

a. An image memory control unit (20a of Fig.3) connected to (see Col.14 line 53 – Col.15 line 4),

b. An image reader (20 of Fig.3) that reads image data (see Col.14 line 53 – Col.15 line 4) and/or an image writer (70 of Fig.3) that writes image data onto a transcription sheet (see Col.18 lines 55-66),

c. An image processing unit (64 of Fig.3) that carries out an image processing of image data such as an editing of image data (see Col.15 lines 59-61 and Col.16 lines 17-57),

d. That receives at least second image data out of first image data that has been read by the image reader (see Col.15 lines 59-61 and Col.16 lines 17-57), and said second image data that has been image processed by the image processing unit (see Col.16 lines 34-57). Here, the image processing unit (64 of Fig.3) can receive data from the image reader (20 of Fig.3), data read from the image memory control unit (which gets its data from the image reader), or from the image processing unit itself, which requires the image processor to make multiple scans of the data in order to completely interpolate it (see Col.16 lines 34-57).

e. That stores at least the second image data out of the first image data and the second image data, into an image memory (55 of Fig.3), and transmits the image

data stored in the image memory to the image processing unit and/or the image writer (70 of Fig.3). Here, while not shown explicitly, there is inherently a buffer (memory) in the printer controller (55 of Fig.3) so that data that is transmitted to it can be held and converted to a printable format (see Col.18 lines 55-66).

f. Wherein at least the image processing unit (64 of Fig.3) has a processor to perform image processing (see Col.15 lines 59-61 and Col.16 lines 17-57).

44. Suguira has not explicitly taught wherein at least the image processing unit has a SIMD type processor.

45. However, Morton has taught a SIMD type processor (see Col.5 lines 37-40) for improving the performance of image processing (see Col.1 lines 18-38) comprising:

a. A parallel processing unit (see 110-113 of Fig.1) that carries out a parallel processing using a plurality of arithmetic units which carry out an arithmetic processing to given data (see Col.24 lines 24-30),

b. A data providing unit (109 of Fig.1) that provides data to be arithmetically processed to the parallel processing unit (see Col.21 lines 40-53),

c. An instruction providing unit (105 of Fig.1) that provides the same instruction for carrying out the arithmetic processing to each of the arithmetic unit (see Col.16 line 34 – Col.17 line 24),

d. An input unit (106 of Fig.1) that inputs an interruption request for carrying out other parallel processing by interrupting a parallel processing currently carried out by the parallel processing unit (see Col.17 line 37 – Col.18 line 8),

e. A decision unit (106 of Fig.1) that makes a decision as to whether a parallel processing requested by the interruption request input from the input unit is to be carried out or not (see Col.17 lines 54-59). Here, the interrupt controller makes a decision whether to process an interrupt based on its priority.

f. A suspending (106 of Fig.1) unit that suspends a parallel processing currently being carried out by the parallel processing unit when the decision unit has decided that the interruption processing is to be carried out (see Col.17 lines 60-66),

g. A control unit (106 of Fig.1) that controls the data providing unit and the instruction providing unit so as to provide data to be arithmetically processed by the interruption processing to the parallel processing unit in place of the parallel processing suspended by the suspending unit and to provide the same instruction necessary for carrying out the interruption processing to each of the arithmetic units (see Col.17 line 54 – Col.18 line 8). Here, an interrupt vector is loaded and subsequently executed following the suspension of the normal execution.

46. Therefore, one of ordinary skill in the art would have found it obvious to modify the image processor of Sugiura to be a SIMD type processor as taught by Morton so that the image processing that Suguira performs can performed at a much faster rate.

47. Claim 29 is nearly identical to claim 8. Claim 8 requires that the image processing unit have a SIMD type processor, while claim 29 requires that the image processing unit has a parallel processing apparatus. However, a SIMD type processor is a parallel processing

apparatus (see Col.5 lines 37-40 and Col.24 lines 24-30). Therefore, claim 29 is rejected for the same reasons as claim 8.

48. Regarding claims 9 and 30, taking claim 9 as exemplary, Suguira in view of Morton has taught the image processing apparatus according to claim 8, wherein:

a. The image memory control unit (Suguira, 20a of Fig.3) is connected to the image processing unit (Suguira, 64 of Fig.3), the image reader (Suguira, 20 of Fig.3) and/or the image writer (Suguira, 70 of Fig.3) via the image data control unit (Suguira, 50 of Fig.3) (see Suguira, Fig.3 for connections),

b. The image data control unit (Suguira, 50 of Fig.3) transmits and receives image data between the image memory control unit (Suguira, 20a of Fig.3), the image processing unit (Suguira, 64 of Fig.3), the image reader (Suguira, 20 of Fig.3) and/or the image writer (Suguira, 70 of Fig.3) (see Suguira, Fig.3 for data flow directions).

49. Claim 30 is nearly identical to claim 9, differing in its parent claim, but encompassing the same scope as claim 9. Therefore, claim 30 is rejected for the same reasons as claim 9.

50. Regarding claims 10 and 31, taking claim 10 as exemplary, Suguira has taught the image processing apparatus comprising:

a. An image processing unit (64 of Fig.3) that is connected to an image reader (20 of Fig.3) that reads image data and/or image memory (59 of Fig.3), a control unit (50 of Fig.3) that controls an image memory to write/read image data (see Col.15 lines 46-49) and/or an image writer (70 of Fig.3) that writes image data onto a transcription sheet (see Col.18 lines 55-66),

b. That receives first image data that has been read by the image reader (see Col.15 lines 59-61 and Col.16 lines 17-57) and/or second image data that has been read by the image memory control unit (20a of Fig.3). Here, the image processing unit (64 of Fig.3) can receive data from the image reader (20 of Fig.3), or from the data read from the image memory control unit, which gets its data from the image reader (see Fig.3).

c. That carries out an image processing of the first image data and/or the second image data such as an editing of image data (see Col.15 lines 59-61 and Col.16 lines 17-57, and transmits the image-processed image data to the image memory control unit and/or the image writer (see Col.18 lines 55-66). Here, because the claim is written in the alternative format, Suguira has met the limitation because the image processing unit (64 of Fig.3) of Suguira transmits the image-processed data to the image writer (see Fig.3 and Col.18 lines 55-66).

d. Wherein at least the image processing unit has a processor (see Col.15 lines 59-61 and Col.16 lines 17-57).

51. Suguira has not explicitly taught wherein at least the image processing unit has a SIMD type processor.

52. However, Morton has taught a SIMD type processor (see Col.5 lines 37-40) for improving the performance of image processing (see Col.1 lines 18-38) comprising:

a. A parallel processing unit (see 110-113 of Fig.1) that carries out a parallel processing using a plurality of arithmetic units which carry out an arithmetic processing to given data (see Col.24 lines 24-30),

b. A data providing unit (109 of Fig.1) that provides data to be arithmetically processed to the parallel processing unit (see Col.21 lines 40-53),

c. An instruction providing unit (105 of Fig.1) that provides the same instruction for carrying out the arithmetic processing to each of the arithmetic unit (see Col.16 line 34 – Col.17 line 24),

d. An input unit (106 of Fig.1) that inputs an interruption request for carrying out other parallel processing by interrupting a parallel processing currently carried out by the parallel processing unit (see Col.17 line 37 – Col.18 line 8),

e. A decision unit (106 of Fig.1) that makes a decision as to whether a parallel processing requested by the interruption request input from the input unit is to be carried out or not (see Col.17 lines 54-59). Here, the interrupt controller makes a decision whether to process an interrupt based on its priority.

f. A suspending (106 of Fig.1) unit that suspends a parallel processing currently being carried out by the parallel processing unit when the decision unit has decided that the interruption processing is to be carried out (see Col.17 lines 60-66),

g. A control unit (106 of Fig.1) that controls the data providing unit and the instruction providing unit so as to provide data to be arithmetically processed by the interruption processing to the parallel processing unit in place of the parallel processing suspended by the suspending unit and to provide the same instruction necessary for carrying out the interruption processing to each of the arithmetic

units (see Col.17 line 54 – Col.18 line 8). Here, an interrupt vector is loaded and subsequently executed following the suspension of the normal execution.

53. Therefore, one of ordinary skill in the art would have found it obvious to modify the image processor of Sugiura to be a SIMD type processor as taught by Morton so that the image processing that Suguira performs can performed at a much faster rate.

54. Claim 31 is nearly identical to claim 10. Claim 10 requires that the image processing unit have a SIMD type processor, while claim 31 requires that the image processing unit has a parallel processing apparatus. However, a SIMD type processor is a parallel processing apparatus (see Col.5 lines 37-40 and Col.24 lines 24-30). Therefore, claim 31 is rejected for the same reasons as claim 10.

55. Regarding claims 11 and 32, taking claim 11 as exemplary, Suguira in view of Morton has taught the image processing apparatus according to claim 10, wherein:

a. The image processing unit (Suguira, 64 of Fig.3) is connected to the image reader (Suguira, 20 of Fig.3) and/or the image memory control unit (Suguira, 20a of Fig.3) and/or the image writer (Suguira, 70 of Fig.3) via the image data control unit (Suguira, 50 of Fig.3) (see Suguira, Fig.3 for connections),

b. The image data control unit (Suguira, 50 of Fig.3) transmits and receives image data between the image processing unit (Suguira, 64 of Fig.3), the image reader (Suguira, 20 of Fig.3) and/or the image memory control unit (Suguira, 20a of Fig.3) and/or the image writer (Suguira, 70 of Fig.3) (see Suguira, Fig.3 for data flow directions).

56. Claim 32 is nearly identical to claim 11, differing in its parent claim, but encompassing the same scope as claim 11. Therefore, claim 32 is rejected for the same reasons as claim 11.

57. Regarding claims 12-14 and 33-35, taking claim 12 as exemplary, Suguira in view of Morton has taught the image processing apparatus according to claim 7, further comprising:

a. A facsimile control unit (Suguira, 54 of Fig.3) that is connected to the image memory control unit and/or the image data control unit (see Suguira, Fig.3), and that carries out transmission and reception of a facsimile image (see Suguira, Col.16 line 61 – Col.17 line 15).

58. Claims 13-14 and 33-35 are nearly identical to claim 12, differing in their parent claims, but encompassing the same scope as claim 12. Therefore, claims 13-14 and 33-35 are rejected for the same reasons as claim 12.

59. Regarding claims 15-17 and 36-38, taking claim 15 as exemplary, Suguira in view of Morton has taught the image processing apparatus according to claim 7, wherein the image reader (Suguira, 20 of Fig.3) and/or the image data control unit (Suguira, 50 of Fig.3) and/or the image memory control unit (Suguira, 20a of Fig.3) and/or the image processing unit (Suguira, 64 of Fig.3) and/or the image writer (Suguira, 70 of Fig.3) and/or the facsimile control unit (Suguira, 54 of Fig.3) are structure as independent units respectively.

60. Claims 16-17 and 36-38 are nearly identical to claim 15, differing in their parent claims, but encompassing the same scope as claim 15. Therefore, claims 16-17 and 365-38 are rejected for the same reasons as claim 15.

61. Regarding claims 19-21 and 40-42, taking claim 20 as exemplary, Morton has taught a SIMD type processor, said SIMD type processor (see Col.5 lines 37-40) comprising:

a. A parallel processing unit (see 110-113 of Fig.1) that carries out a parallel processing using a plurality of arithmetic units which carry out an arithmetic processing to given data (see Col.24 lines 24-30),

b. A data providing unit (109 of Fig.1) that provides data to be arithmetically processed to the parallel processing unit (see Col.21 lines 40-53),

c. An instruction providing unit (105 of Fig.1) that provides the same instruction for carrying out the arithmetic processing to each of the arithmetic unit (see Col.16 line 34 – Col.17 line 24),

d. An input unit (106 of Fig.1) that inputs an interruption request for carrying out other parallel processing by interrupting a parallel processing currently carried out by the parallel processing unit (see Col.17 line 37 – Col.18 line 8),

e. A decision unit (106 of Fig.1) that makes a decision as to whether a parallel processing requested by the interruption request input from the input unit is to be carried out or not (see Col.17 lines 54-59). Here, the interrupt controller makes a decision whether to process an interrupt based on its priority.

f. A suspending (106 of Fig.1) unit that suspends a parallel processing currently being carried out by the parallel processing unit when the decision unit has decided that the interruption processing is to be carried out (see Col.17 lines 60-66),

g. A control unit (106 of Fig.1) that controls the data providing unit and the instruction providing unit so as to provide data to be arithmetically processed by the interruption processing to the parallel processing unit in place of the parallel

processing suspended by the suspending unit and to provide the same instruction necessary for carrying out the interruption processing to each of the arithmetic units (see Col.17 line 54 – Col.18 line 8). Here, an interrupt vector is loaded and subsequently executed following the suspension of the normal execution.

62. Morton has not explicitly taught the SIMD type processor being comprised in a printer, a facsimile machine, or a scanner.

63. However, Sugiura has taught a facsimile machine (see Sugiura, Col.5 lines 11-21), which also comprises a scanner (image reader, see Sugiura, 20 of Fig.3) and a printer (laser printer, see Sugiura, 70 of Fig.3), which uses a processor for image processing (see Sugiura, 64 of Fig.3 and Col.15 lines 59-61 and Col.16 lines 17-57). Because Morton has taught an SIMD processor (see Morton, Col.5 lines 37-40) for improving the performance of image processing (see Morton, Col.1 lines 18-38), one of ordinary skill in the art would have found it obvious to modify the processor of Morton to be comprised in a facsimile machine, that also comprises a scanner and a printer, so that image processing performance can be improved.

64. Claims 19, 21 and 40-42 are nearly identical to claim 20. Claims 19 and 40 differ in that the SIMD processor is being comprised in a printer. However, the facsimile machine of Suguira also comprises a printer (see Sugiura, 70 of Fig.3). Claims 21 and 42 differ in that the SIMD processor is being comprised in a scanner. However, the facsimile machine of Suguira also comprises a scanner (see Sugiura, 20 of Fig.3). Claim 41 differs in the limitations being comprised within a parallel processing apparatus instead of a SIMD type processor as recited in claim 20. However, a SIMD type processor is a parallel processing apparatus (see Morton, Col.5

lines 37-40 and Col.24 lines 24-30). Therefore, claims 19, 21 and 40-42 are rejected for the same reasons as claim 20.

65. Regarding claims 45 and 49, taking claim 45 as exemplary, Suguira has taught an image processing method comprising:

a. An image data receiving step of receiving image data from any one processing unit (64 of Fig.3) out of a plurality of processing units (see Fig.3) that carry out different kinds of processing of image data such as an image data reading processing, an image data storing processing, an image (editing) processing, and a transmission/reception processing (see Col.15 lines 59-61 and Col.16 lines 17-57),

b. An image data control information obtaining step of obtaining image data control information that includes information relating to the contents of processing of the image data received at the image data receiving step (see Col.15 lines 46-49 and Col.16 lines 4-16),

c. A transmission destination processing unit determining step of determining a processing unit at a transmission destination to which the image data received at the image data receiving step is to be transmitted, based on the image data control information obtained at the image data control information obtaining step (see Col.18 line 55 – Col.19 line 12). Here, the MPU determines whether the image data is to be output to the printer or to another facsimile machine.

d. A transmission step of transmitting the image data to the transmission destination processing unit that has been determined at the transmission destination

processing unit determining step (see Col.18 line 55 – Col.19 line 12). Here, based on its determination, the MPU transmits the image data to the printer or to the other facsimile machine.

e. Wherein the processing of the image data in at least one processing unit among the plurality of processing units includes a processing method (see Col.15 lines 59-61 and Col.16 lines 17-57).

66. Suguira has not explicitly taught wherein the processing of the image data in at least one processing unit among the plurality of processing units includes a parallel processing method.

67. However, Morton has taught a parallel processing method for improving the performance of image processing (see Col.1 liens 18-38) comprising:

I. A data providing step of providing data to be processed as a parallel processing (see Col.21 lines 40-53),

II. An instruction providing step of providing an instruction necessary for carrying out the parallel processing (see Col.16 line 34 – Col.17 line 24),

III. A parallel-processing step of carrying out a parallel processing of the data provided at the data providing step, based on the instruction provided at the instruction providing step (see Col.24 lines 24-30),

IV. An input step of inputting an interruption request for carrying out other parallel processing currently carried out at the parallel-processing step (see Col.17 line 37 – Col.18 line 8),

V. A decision step of making a decision as to whether an interruption processing of the parallel processing requested at the input step is to be

carried out or not (see Col.17 lines 54-59). Here, the interrupt controller makes a decision whether to process an interrupt based on its priority.

VI. A suspending step of suspending a parallel processing currently being carried out at the parallel-processing step when a decision has been made at the decision step that the interruption processing is to be carried out (see Col.17 lines 60-66),

VII. A replacing step of providing data to be parallel processed by the interruption processing and an instruction necessary for carrying out the interruption processing, in place of the parallel processing suspended at the suspending step (see Col.17 line 54 – Col.18 line 8). Here, an interrupt vector is loaded and subsequently executed following the suspension of the normal execution.

68. Therefore, one of ordinary skill in the art would have found it obvious to modify the image processing method of Sugiura to be a parallel image processing method as taught by Morton so that the image processing of Suguira can be performed at a much faster rate.

69. Claim 49 is nearly identical to claim 45. Claim 49 differs in the limitations being comprised on a computer readable medium, but Morton has taught its instructions being stored on a computer readable medium for executing (see Col.6 lines 33-45 and Col.14 lines 39-61). Therefore, claim 49 is rejected for the same reasons as claim 45.

70. Regarding claim 46, Suguira in view of Morton has taught the image processing method according to claim 45, further comprising:

a. A control information input step of inputting the image data control information (see Col.15 lines 46-49 and Col.16 lines 4-16),

b. Wherein at the image data control information obtaining step, the image data control information input at the control information input step is obtained (see Col.15 lines 46-49 and Col.16 lines 4-16).

71. Regarding claim 47, Suguira in view of Morton has taught the image processing method according to claim 45, wherein the image processing method is used for a correction processing for correcting information deterioration of image data or a picture quality processing corresponding to image data corrected by the correction processing or image data corresponding to an image forming characteristic (see Col.16 lines 34-57 and Col.22 lines 18-52).

72. Claims 18 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morton, U.S. Patent No. 6,088,783, in further view of Ojha, U.S. Patent No. 5,274,468.

73. Regarding claims 18 and 39, taking claim 18 as exemplary, Morton has taught a SIMD type processor, said SIMD type processor (see Col.5 lines 37-40) comprising:

a. A parallel processing unit (see 110-113 of Fig.1) that carries out a parallel processing using a plurality of arithmetic units which carry out an arithmetic processing to given data (see Col.24 lines 24-30),

b. A data providing unit (109 of Fig.1) that provides data to be arithmetically processed to the parallel processing unit (see Col.21 lines 40-53),

c. An instruction providing unit (105 of Fig.1) that provides the same instruction for carrying out the arithmetic processing to each of the arithmetic unit (see Col.16 line 34 – Col.17 line 24),

d. An input unit (106 of Fig.1) that inputs an interruption request for carrying out other parallel processing by interrupting a parallel processing currently carried out by the parallel processing unit (see Col.17 line 37 – Col.18 line 8),

e. A decision unit (106 of Fig.1) that makes a decision as to whether a parallel processing requested by the interruption request input from the input unit is to be carried out or not (see Col.17 lines 54-59). Here, the interrupt controller makes a decision whether to process an interrupt based on its priority.

f. A suspending (106 of Fig.1) unit that suspends a parallel processing currently being carried out by the parallel processing unit when the decision unit has decided that the interruption processing is to be carried out (see Col.17 lines 60-66),

g. A control unit (106 of Fig.1) that controls the data providing unit and the instruction providing unit so as to provide data to be arithmetically processed by the interruption processing to the parallel processing unit in place of the parallel processing suspended by the suspending unit and to provide the same instruction necessary for carrying out the interruption processing to each of the arithmetic units (see Col.17 line 54 – Col.18 line 8). Here, an interrupt vector is loaded and subsequently executed following the suspension of the normal execution.

74. Morton has not explicitly taught the SIMD type processor being comprised in a printer, a facsimile machine, or a scanner.

75. However, Ojha has taught a copier (see Ojha, Col.4 lines 9-28), which uses a processor for image processing (see Ojha, Col.4 lines 29-41). Because Morton has taught an SIMD

processor (see Morton, Col.5 lines 37-40) for improving the performance of image processing (see Morton, Col.1 lines 18-38), one of ordinary skill in the art would have found it obvious to modify the processor of Morton to be comprised in a copier, so that image processing performance of the copier could be improved.

Conclusion

76. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

77. Hung et al., U.S. Patent No. 6,530,010 has taught a SIMD processor for image and digital signal processing functions.

78. Taylor et al., U.S. Patent No. 5,463,732 has taught a SIMD processing system for image processing.

79. Barry et al., U.S. Patent Publication 2001/0049763 has taught an SIMD processor with explicit interrupt handling capabilities.

80. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

81. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
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